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ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
Suite 600
1050 Connecticut Ave, N.W.
Washington, DC 20036-5339

EXAMINER
ENGLUND, TERRY LEE

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/769,534	AKIYOSHI, HIDEO	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12 and 17* is/are allowed.

6)☒ Claim(s) *1-3,5,7-11,13,15 and 18-20* is/are rejected.

7)☒ Claim(s) *4,6,14 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

The amendment submitted on Mar 3, 2003 was reviewed and considered with the following results:

The amended claims overcame the rejections of claims 8, 11, 14, and 16 under 35 U.S.C. 112 as described in the previous Office Action. Those rejections have been withdrawn. However, newly added claims 18 and 20 have their own respective problems, which are described later under the appropriate section.

The amended claims and/or comments also overcame all their prior art rejections as described in the previous Office Action. Those rejections include: 1) claims 1-11 under 35 U.S.C. 102(e) with respect to Malherbe; 2) claims 1-3, 5, 7-12, and 17 under 35 U.S.C. 102(e) with respect to Crotty; 3) claims 13-16 under 35 U.S.C. 103(a) with respect to Malherbe; and 4) claims 13-16 under 35 U.S.C. 103(a) with respect to Crotty. Neither Malherbe nor Crotty clearly show or disclose a pulse including at least one rectangular pulse as now recited within each of the amended independent claims. [It is understood a pulse can simply be a transition from a low to high logic level (or vice versa), but this simple pulse does not have a rectangular pulse as understood from the comments, disclosure and figures. Unless the simple transition pulse also includes at least one pulse with corresponding rising and falling edges, the simple pulse does not meet the "rectangular pulse" limitation now recited. For example, each of the PLSH and POR pulses in the applicant's Fig. 3 shows a transition from a low to high logic level, and also clearly show at least one rectangular pulse (i.e. having one leading edge and one trailing edge) within the low to high pulse.] Since neither reference clearly shows or describes an external power-on

reset signal as being supplied from the exterior of the IC as recited within claims independent 13 and 15, those claims have been withdrawn. Although all of the prior art rejections described in the previous Office Action have now been withdrawn, a new search found several references that are deemed to read on at least some of the claimed inventions. Along with the new rejections, several withdrawn rejections (based on previously cited prior art references) have been modified, and all of these rejections are described in their appropriate section later.

Claim Rejections under 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 18 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Claim 18, line 8 "having pulses" implies the main power-on reset signal always has at least two pulses. Since the applicant's own Fig. 3 waveform (m) shows only a single (rectangular) pulse, it is not clear if the applicant means the low to high transition is deemed one pulse, and the rectangular pulse is another pulse. However, it is also possible to interpret claim 18's "having pulses" phrase as attempting to refer to at least two rectangular type pulses. Therefore, correction and/or clarification are required with respect to what "having pulses" means within claim 18. Also related to these pulses within claim 18, it is not clear how they can correspond to "each of said sub power-on reset signals" if the main power-on reset signal can be generated according to only one of the sub power-on reset signals as recited on lines 4-6 (i.e. "at least one of said...signals"). It is not clear in claim 20 what the applicant refers to by "having pulses not overlapping" as recited on line 8. For example, if the applicant's own

signals PLSH and PLSL (shown in Fig. 3) are deemed the pulse signals as power-on reset signals, their main low-to-high transition pulses clearly overlap. However, if only the rectangular pulses are to be considered, these pulse types are not clearly identified within the claims 18 and 20.

Claim Rejections under 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 7, and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Zhou et al. (Zhou), a reference found during a recent search. Fig. 5 shows a sub reset signal generator 120,520,530 for generating a plurality of sub power-on reset signals NODE C and NODE D having different timings (see Figs. 6(D) and 6(E), respectively); and a main reset signal generator 540,550 for generating a pulse signal POR including at least one rectangular pulse (see the pulse between T11 and T14 in Fig. 6(F)) as the main power-on reset signal POR to initialize an internal circuit (e.g. see 110 of Fig. 1). Signal POR is according to at least one from any of the sub power-on reset signals, thus anticipating claim 1. Interpreting Fig. 5 slightly differently, 120,522 can be deemed a sub reset signal generator for generating a plurality of sub power-on reset signals POR1,NODE A with different timings (see Figs. 6(A) and 6(B)); and a main reset signal generator 524-550 for generating pulse signal POR as the main power-on reset signal to initialize the internal circuit, anticipating claim 1. The main reset signal generator comprises a

plurality of signal generators 524-529,530 for generating pulses NODE C,NODE D on the basis of transitions of their corresponding sub power-on reset signals (see Fig. 6), and a composite circuit 540,550 for synthesizing the pulses to generate signal POR, anticipating claim 2. Also be interpreting the figures differently, power-on reset pulse signals NODE C and NODE D are generated according to a plurality of sub power-on reset signals NODE B and POR1 having different timings from each other; and it is understood signal POR is used to initialize an internal circuit (e.g. 110 of Fig. 1) according to at least one from any of the signals NODE C and NODE D. As shown in Fig. 6, both NODE C and NODE D have at least one rectangular pulse, anticipating claim 7. 120,522 can be deemed a sub reset signal generator for generating a plurality of sub power-on reset signals POR1 and NODE A with different timings (see Figs. 6(a) and 6(B)); 524-529 and 530 can be deemed a plurality of pulse generators for generating pulses NODE C and NODE D on the basis of NODE A and POR1, respectively wherein both NODE C and NODE D each have a rectangular pulse (see Figs. 6(D) and 6(E)); and composite circuit 540,550 synthesizes pulses NODE C and NODE D to generate main power-on reset signal POR, thus claim 10 is anticipated.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Lee's U.S. Patent 6,492,848 ('848), another reference found during ac recent search. Fig. 4 shows a semiconductor integrated circuit comprising a sub reset signal generator INV41-INV45 for generating a plurality of sub power-on reset signals N45,N46 at timings different from each other (see Fig. 5); and a main reset signal generator XOR41 for generating a pulse signal POR, including at least one rectangular pulse (see Fig. 5), understood to be used as a main power-on reset to initialize an

internal circuit. Since signal POR is generated according to signals N45,N46, claim 1 is anticipated.

Claim Rejections under 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In so far as being understood, claims 8, 9, 11, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou et al. (Zhou). Zhou's Fig. 5 shows a circuit comprising a sub reset signal generator 120,520,530 for generating a plurality of sub power-on reset signals NODE C and NODE D; and main reset signal generator 540,550 generates a pulse signal POR including at least one rectangular pulse (see Fig. 6(F)) according to at least one of said signals NODE C and NODE D. The reference also shows section 120 comprising two transistors (unlabeled) which one of ordinary skill in the art would know have their own respective threshold voltages. However, the reference does not clearly show or disclose the generation of signals NODE C and NODE D on the basis of respective threshold values of the transistors. Since section 120 comprises CMOS transistors, it would have been obvious to one of ordinary skill in the art to form each of the inverters (e.g. 522, 527, 532, 534, and 550) as a CMOS inverter, and each of the logic devices (e.g. 524, 528, and 540) could be formed using appropriate combinations of MOS transistors. Each transistor would have its own respective threshold voltage, and it would be understood the inverters and logic devices would trigger when their threshold voltage would be reached. For example, when the respective transistor

threshold(s) within path 522,524,527, 528 is reached, the appropriate signal NODE C is generated. Therefore, claim 8 is rendered obvious. The delays and logic devices can be formed from appropriate MOS structures, and their threshold values (e.g. triggering levels) would provide the basis of the signals generated. The MOS transistors would correspond to the MOS transistors shown within section 120 (thus having similar operational characteristics with respect to voltage and temperature); would be easier to fabricate on an IC; and consume less power than bipolar transistors. For similar reasons, first sub reset signal generator 520 will generate first sub power-on reset signal NODE C on the basis of a first threshold voltage of a first transistor within generator 520; second sub reset signal generator 530 will generate second sub power-on reset signal NODE D on the basis of a second transistor within generator 530; and main reset signal generator 540,550 will generate pulse signal POR (having a rectangular pulse as shown in Fig. 6(F)) to initialize an internal circuit (e.g. 110 of Fig. 1), rendering claim 9 obvious. As previously described, it would have been obvious to one of ordinary skill in the art to use CMOS inverters for each of the inverters within Zhou's Fig. 5. As such, the last inverter of 120 and inverter 522 generate a plurality of sub power-on reset signals POR1 and NODE A, respectively according to the threshold voltage of their respective transistors; 524-529 and 530 generate a plurality of pulse signals NODE C and NODE D, respectively according to signals NODE A and POR1 (as shown in Fig. 6, all of these signals have timings that are different from each other, and each has a rectangular pulse); and signal POR is used to initialize an internal circuit (e.g. 110 of Fig. 1) according to at least one of signals NODE C and NODE D, rendering claim 11 obvious. The transistors are one well-known means for forming inverters. Using transistors in each of the inverter's within Zhou's Fig. 5, signal POR has what can be deemed two pulses (i.e. one main

low to high transition pulse, and one rectangular pulse between T11 and T14), wherein signal POR corresponds to the sub power-on reset signals (e.g. POR1 and NODE B; or NODE C and NODE D). Since there is no reason to use special transistors, it would be obvious to use normal transistors within the inverters. These transistors would have typical values, thus claim 18 is rendered obvious. Using (typical) transistors within the inverters of Zhou, as previously described, 120,522 generate a plurality of sub power-on reset signals POR1,NODE A according to respective (typical) threshold values of their transistors, wherein the signals have different timings (see Figs. 6(A) and 6(B)). These signals are used to generate a plurality of pulse signals as power-on reset signals NODE C, NODE D, wherein at least some sections of the signals are not overlapping each other. Since signals NODE C and NODE D are used to provide signal POR to initialize an internal circuit, claim 20 is rendered obvious.

Claims 8, 9, and 18 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Lee ('848). Fig. 4 of Lee ('848) shows a circuit comprising a sub reset signal generator INV41-INV45 for generating a plurality of sub power-on reset signals N45,N46; and main reset signal generator XOR41 generates pulse signal POR, including at least one rectangular pulse (see Fig. 5), according to at least one of said signals N45,N46 to initialize an internal circuit (e.g. not shown, but understood by one of ordinary skill in the art). However, the reference does not clearly show or disclose the generation of signals N45,N46 on the basis of respective threshold values of transistors. Since section 430 of Fig. 4 comprises MOS transistors, and Fig. 2 clearly shows a CMOS inverter PM21,NM21, it would have been obvious to one of ordinary skill in the art to replace each of inverters INV41-INV45 of Lee's Fig. 4 with CMOS inverters. Each transistor would have its own respective threshold voltage, and it would be understood the

inverters would trigger when their respective transistor threshold voltages would be reached. Therefore, claim 8 is rendered obvious. The CMOS inverters would correspond to the MOS transistors shown within section 430 (thus having similar operational characteristics with respect to voltage and temperature); would be easy to fabricate on an IC; and consume less power than bipolar transistors. For similar reasons, first sub reset signal generator INV43 will generate first sub power-on reset signal N45 on the basis of a first threshold voltage of a first transistor within generator INV43; second sub reset signal generator INV45 will generate second sub power-on reset signal N46 on the basis of a second transistor within generator INV45; and main reset signal generator XOR41 will generate pulse signal POR (having a rectangular pulse as shown in Fig. 5) to initialize an internal circuit, rendering claim 9 obvious. As understood from the waveforms shown in Fig. 5, the leading and trailing edges of signal POR correspond to the leading edges of signals N45 and N46, respectively. Using CMOS transistors within each inverter, signals N45 and N46 will correspond to their respective transistor threshold values. The reference of Lee does not disclose the transistors shown within the figures (e.g. CMOS inverter PM21,NM21 of Fig. 2) have any special configuration. Therefore, they are considered typical MOS transistors, and the use of CMOS transistors within each of the inverters would obviously use typical transistors (e.g. there is no reason to use anything other than typical CMOS transistors). As such, it would be obvious to one of ordinary skill in the art that the threshold values of those transistors will be typical, rendering claim 18 obvious. The typical MOS transistors used within the inverters will correspond to the other MOS transistors used within Lee's Fig 4 circuit.

Claims 3, 5, 13, 15, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou et al. (Zhou) in view of Lee's U.S. Patent 5,394,104 ('104) cited in the previous Office Action. As previously described with respect to rejections of closely related claims 1, 7, and 10, Zhou's Fig. 5 shows a circuit comprising what can be deemed a sub reset signal generator 520,530 for generating sub power-on reset signals NODE C,NODE D; and a main reset signal generator 540,550 for generating pulse signal POR, including at least one rectangular pulse as a main power-on reset signal (see section T11-T14 of Fig. 6 (F)), to initialize an internal circuit (e.g. 110 of Fig. 1) according to the signals received by generator 540,550. However, the reference does not show or disclose the circuit receiving an external power-on reset signal. Lee ('104) shows and discloses the use of an external power-on reset signal (e.g. see 180 in Figs. 1-3B, and 680 in Fig. 6) as an override reset signal (e.g. see column 1, lines 34-35). Therefore, it would have been obvious to one of ordinary skill in the art to also include an external reset signal to Zhou's generator 540,550, rendering claims 3 and 5 obvious. The external reset signal would provide a means to reset the circuit, if a need arises, without having to completely power down and then re-apply the power to the system/circuit. [For example, a personal computer typically has a manual reset button to restart/reboot if a computer error occurs (e.g. operation hangs up).] A reset terminal of the integrated circuit would receive the external reset signal, to ensure generator 540,550 would have the capability of receiving the external reset signal supplied from the exterior of the IC, thus rendering claims 13, 15, and 19 obvious. The external reset would allow the system/circuit to be reset without the need to turn power completely off.

Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malherbe (a reference cited in the previous Office Action), in view of Lee's U.S. Patent

5,394,104 ('104) also cited in a previous Office Action. Fig. 4 clearly shows a sub reset signal generator CE1-CE3 for generating a plurality of sub power-on reset signals (identified as POR1-PORn, respectively in corresponding Fig. 3), and a main reset signal generator OR for receiving those signals in order to generate a pulse signal POR as a main power-on reset signal, wherein it is understood POR is used to initialize an internal circuit. However, the reference does not clearly show or disclose an external power-on reset signal supplied from the exterior of the IC. Lee ('104) shows and discloses the use of an external power-on reset signal (e.g. see 180 in Figs. 1-3B, and 680 in Fig. 6) as an override reset signal (e.g. see column 1, lines 34-35). Therefore, it would have been obvious to one of ordinary skill in the art to also include a reset terminal as a means to provide an external reset signal (with respect to the IC) to Malherbe's generator OR.. This would render claims 13 and 15 obvious. [It is understood that the sub power-on reset signals will have different timings from each other because of the different configurations of CE1, CE2, and CE3, as shown in Fig. 4.] The external reset signal would provide a means to reset the circuit, if a need arises, without having to completely power down and then re-apply the power to the system/circuit. [For example, a personal computer typically has a manual reset button to restart/reboot if a computer error occurs (e.g. operation hangs up).] The reset terminal of the integrated circuit would receive the external reset signal, to ensure generator OR would have the capability of receiving the external reset signal supplied from the exterior of the IC, allowing the external reset to reset the system/circuit without the need to turn power completely off.

For reasons similar to those previously described, claims 13 and 15 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Crotty (another reference cited in the previous Office Action), in view of Lee's U.S. Patent 5,394,104 ('104). Fig. 6 shows a sub reset

signal generator 630,640,210,220 for generating sub power-on reset signals POR2,POR1 (having different timings from each other due to the different configurations of 210 (see Figs. 3(a)) and 630 (see Fig. 8(a)), wherein main reset signal generator 650 (see Fig. 7) receives those signals to generate pulse signal POR as a main power-on reset signal for initializing an internal circuit. However, the reference does not clearly show or disclose a reset terminal for receiving an external power-on reset signal supplied from the exterior of the IC. For the same reasons as applied to the other references described above, it would have been obvious to one of ordinary skill in the art to add a reset terminal to the circuit of Crotty to receive an external power-on reset signal, thus allowing generator 650 to provide the signal POR according to at least one of the POR1, POR2, and the external power-on reset signal, rendering claims 13 and 15 obvious. The external power-on reset signal would provide a means to reset the system/circuit without the need to turn power completely off, if that is desired.

Allowable Subject Matter

Claims 12 and 17 are allowable. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure the generated pulses are shorter than an interval related to the sub power-on reset signals as recited within claims 12 and 17.

Claims 4, 6, 14, and 16 are only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure the main reset signal generator includes a plurality of pulse generators for generating pulses corresponding to the sub power-on reset signal(s) and the external power-on reset signal as recited within claims 4, 6, 14, and 16.

Response to Arguments

The applicant's arguments (within the amendment filed Mar 3, 2003), with respect to the rejection of claims 1-17, have been fully considered and were found persuasive at least in part. Therefore, those rejections have been withdrawn as previously described due to the amended sections of the claims and/or related arguments. However, the following comments relate to the arguments, and the examiner's interpretations of the references and claimed limitations.

Although pages 8 and 11 of the amendment both imply the main power-on reset signals of claims 1, 3, 5, and 7-11 have at least one rectangular pulse, only claims 1, 3, 5, 8 and 9 actually recite it clearly. Claims 7, 10, and 11 only indicate at least one pulse (signal) includes a rectangular pulse, without identifying that pulse (signal) as the main power-on reset signal.

Pages 8 and 10 of the amendment indicate the references of Malherbe and Crotty do not disclose a reset terminal for receiving an external power-on reset signal as recited within claims 3 and 5. However, those claims do not clearly identify what the applicant means by external. For example, Malherbe's Fig. 3 shows DET providing TPOR to OR, wherein DET is separated from CE1-Cen,OR by a dashed line. Therefore, under the broadest reasonable interpretation of an external power-on reset signal, DET can still be deemed to be external to all of the other elements shown, without being external to the IC itself. Similarly, Crotty's test circuit 1020 can be considered external to all the other elements shown in Fig. 10. Since claims 13 and 15 do recite the external power-on reset signal is supplied from the exterior of the IC, those rejections have been withdrawn, but modified rejections of those claims have been provided within this action.

Page 10 states POR1 of Crotty is not a pulse signal. However, a transition from a logic low to a logic high, or vice versa, can be deemed one type of pulse signal. Also, it is known that an output of a logic gate (e.g. NAND 410 of Crotty's Fig. 4(a)) is a pulse. Only by indicating the pulse signal includes a rectangular pulse does the claimed limitation read over Crotty's circuit. [Since Crotty's delay includes an even number of inverters, the Fig. 4(a) circuit will not function as a one-shot pulse generator as the examiner had initially believed. It will merely provide one logic transition as output signal POR1 unless input VD1 periodically varies above and below the trigger level of the delay and logic gate.]

The comments on page 10 with respect to Crotty's buffer circuit 650 (shown in Fig. 7) being an AND gate, and that POR signals having pulses cannot be generated from the POR1 signal is not clearly understood. The applicant's own composite circuit 20 (e.g. see the applicant's Figs. 1 and 4) comprise the same configuration, wherein a multi-input NAND gate and an inverter are coupled in series. One of ordinary skill in the art knows that unless both (or all of) the input signals are high, the output of the NAND gate will be low. When all of the input signals become high, the gate's output will become (i.e. pulse) high.

The footnote on page 10 indicates the reference of Lee also does not have the reset circuit outside the IC. However, the claims do not recite any type of reset circuit being external to the IC. The claims merely recite that an external power-on reset signal is received. Therefore, one of ordinary skill in the art could reasonably interpret this as meaning any type of reset signal (e.g. one applied manually or automatically), received from the outside of the circuit, can be deemed an external power-on reset signal.

It is believed the rejections described in this Office Action are proper with respect to the interpretation of the claimed limitations, and the prior art references cited.

The applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). The applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for TC 2800 is (703) 872-9318 for communications before a final action has been mailed, and (703) 872-9319 for communications after a final action.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

TLE

Terry L. Englund
12 May 2003

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800